REMARKS

Claims 1-20 are all the claims presently pending in the application. Claims 1 and 10 are independent.

Applicants appreciate the courtesies extended to the Applicants' representative during the personal interview on May 13, 2004. During the personal interview, Examiner Nguyen agreed that the Yamashita et al. reference does not teach or suggest the feature of a serpentine channel region.

Applicants note that, notwithstanding any claim amendments herein or later during prosecution, Applicants' intent is to encompass equivalents of all claim elements.

Entry of this Request for Reconsideration is proper. Since the claimed features and their distinctions over the prior art of record were discussed earlier, and since no further amendments are being made to the claims, this paper does not raise a new issue requiring a further search and/or consideration by the Examiner.

Claims 1-20 stand rejected under 35 U.S.C. 112, second paragraph. Claims 1-2 stand rejected under 35 U.S.C. 102(b) as being anticipated by the Yamashita, et al. reference (USPN 5,506,516).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

A first exemplary embodiment of the claimed invention, as defined by independent claim 1, is directed to a display system that includes an array of pixel cells formed on a substrate. Each

pixel cell being coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. The device includes a first and second transistor formed on the substrate each having a gate electrode and first and second electrodes defining a serpentine channel region there between.

A second exemplary embodiment of the claimed invention, as defined by independent claim 10, is directed to a display system that includes an array of pixel cells formed on a substrate. Each pixel cell being coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. The system further includes a gate line select/hold circuit formed on the substrate and connected to at least one of the plurality of gate lines, a first control pad and a first probe pad, and a data line select/hold circuit formed on the substrate and connected to at least one of said plurality of data lines, a second control pad and a second probe pad. At least one of the gate line select/hold circuit and the data line select/hold circuit includes first and second transistors each having first and second electrodes defining a serpentine channel region.

Conventional display systems include pixel cells formed on a substrate which are each coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. An array tester provides a means for testing the cells of such a display system by coupling probes to gate line pads and data line pads that terminate the gate lines and data lines, respectively. In other words, the array tester is coupled directly to each gate line and each data line. However, when the size of such a conventional display system is changed the spacing of the gate lines and/or data lines also

changes which requires that the probe fixture of the array tester be modified to accommodate these changes.

By contrast, the present invention includes first and second electrodes in addition to the pixel array which accommodate variations in size and/or resolution without requiring modification of the probe fixture of the array tester. In other words, the present invention provides a flexible interface between the array under test and the test system. More specifically, in the event that the size of the array under test is changed, the gate line select/hold circuit 17 and/or the data line select/hold circuit 19 and the probe pads associated therewith may be designed such that they align with the spacing of an existing probe fixture, thereby eliminating the high costs associated with redesigning the probe fixture of the array.

Further, each of the first and second transistors have a gate electrode and first and second electrodes defining a serpentine channel region. This feature minimizes the time constant required to transfer a charge to/from a capacitive load using the select and hold transistors of the gate line select/hold circuit 17 and the data line select/hold circuit 19 and also reduces the ON resistance of these transistors. The ON resistance of the transistor is proportional to the channel length/width ratio of the transistor. The serpentine channel region minimizes this length/width ratio and, therefore, reduces the ON resistance and the time constant.

Exemplary embodiments of serpentine channel regions are illustrated by Figure 10(B) and is described in the specification at, for example, page 20, line 20 - page 21, line 8. In particular, Figure 10(B) illustrates a serpentine channel region between electrodes A and C of the select transistor and another serpentine region between electrodes C and E of the hold transistor.

These serpentine channel regions along with their advantages were explained to Examiner Nguyen by the Applicants' representative during the May 13, 2004 personal interview.

II. THE 35 U.S.C. § 112, SECOND PARAGRAPH REJECTION

The Examiner alleges that claims 1-20 is indefinite. In particular, the Office Action alleges that claims 1 and 10 are indefinite.

However, in view of the explanation by Applicants' representative during the May 13, 2004 personal interview, the "Examiner also agrees to withdraw the rejection of claims 1 and 10 under 35 U.S.C. § 112, 2nd paragraph based upon Mr. Howard's remarks about figure 10(b)." (Examiner's Interview Summary).

II. THE PRIOR ART REJECTION

Regarding the rejection of claims 1-2, the Office Action alleges that the Yamashita et al. reference teaches the claimed invention. Applicants submit, however, that there are elements of the claimed invention which are neither taught nor suggested by the Yamashita et al. reference.

As explained in the Remarks from the Amendment that was filed on December 1, 2003, the Yamashita et al. reference does not teach or suggest the features of the claimed invention including a serpentine channel region. As explained above, this feature minimizes the time constant required to transfer a charge to/from a capacitive load using the select and hold transistors of the gate line select/hold circuit 17 and the data line select/hold circuit 19 and also reduces the ON resistance of these transistors. The ON resistance of the transistor is proportional

to the channel length/width ratio of the transistor. The serpentine channel region minimizes this length/width ratio and, therefore, reduces the ON resistance and the time constant.

Indeed, the Applicants pointed out to the Examiner that the Examiner failed to present a prima facie case of anticipation by failing to point out with particularity where the Examiner contends that a serpentine channel region is disclosed by the Yamashita et al. reference.

During the personal interview on May 13, 2004, the Examiner explained that he had not reviewed the present specification and did not understand that Figure 10(B) illustrated an exemplary embodiment of a serpentine channel region. Rather, Examiner Nguyen explained that he was under the impression that the schematic representation of the select/hold transistor pair of Fig. 10(A) illustrated a serpentine channel region as a line that extends, for example, from the node "A" to the node "C." Examiner Nguyen then explained that the Yamashita et al. reference illustrates the same type of schematic representation of transistors.

Applicants' representative explained that Figure 10(A) is merely a symbolic representation of a select/hold transistor pair and does not illustrate the actual structure of the select/hold transistor pair. Rather, Figure 10(A) is merely a schematic representation.

In stark contrast, Figure 10(B) illustrates an exemplary embodiment of the actual structure of electrodes of a select/hold transistor pair that includes serperntine channel regions. As explained above, Figure 10(B) illustrates a serpentine channel region between electrodes A and C of the select transistor and another serpentine region between electrodes C and E of the hold transistor.

Examiner Nguyen then agreed that "Yamashita et al. do (sic) not disclose a serpentine

channels (sic) as shown in figure 10(b)."(Examiner's Interview Summary).

Therefore, Examiner Nguyen agrees that the Yamashita et al. reference does not teach or suggest each and every element of the claimed invention and Applicants respectfully request that the Examiner withdraw this rejection of claims 1-2.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing remarks, and in light of the agreement that was reached during the personal interview, Applicants respectfully submit that claims 1-20, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 5/17/04

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this After-Final Request for Reconsideration by facsimile with the United States Patent and Trademark Office to Examiner Venh P. Nguyen, Group Art Unit 2829 at fax number (703) 872-9306 this 17th day of May, 2004.

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